

FINAL



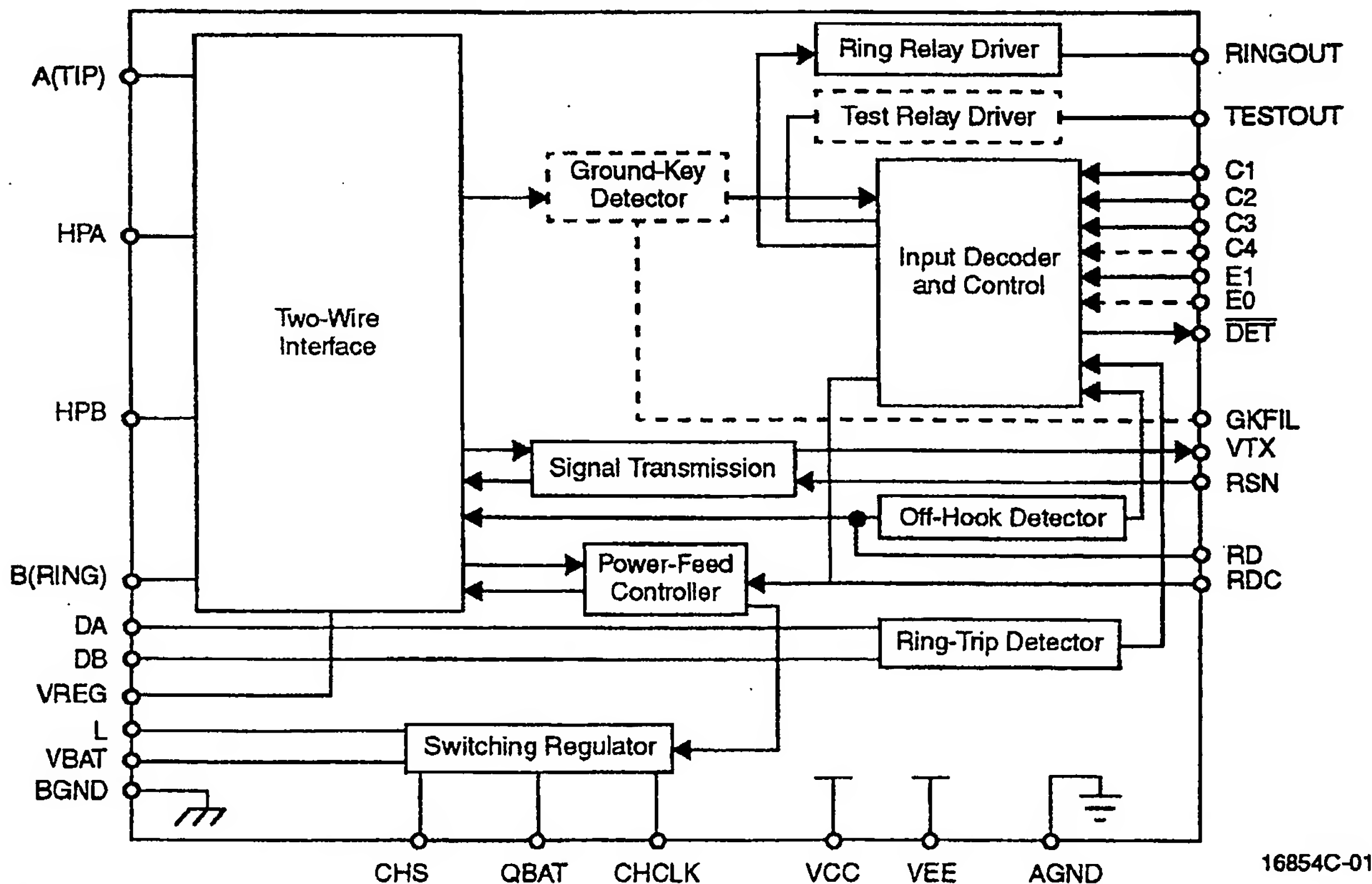
# Am79530/Am79531/Am79534/Am79535

## Subscriber Line Interface Circuit

### DISTINCTIVE CHARACTERISTICS

- Programmable constant-current feed
- Line-feed characteristics independent of battery variations
- Programmable loop-detect threshold
- On-chip switching regulator for low-power dissipation
- Pin for external ground-key noise-filter capacitor available
- Ground-key detect
- Two-wire impedance set by single external impedance
- Polarity reversal feature
- Tip Open state for ground-start lines
- Test relay driver optional
- On-hook transmission

### BLOCK DIAGRAM



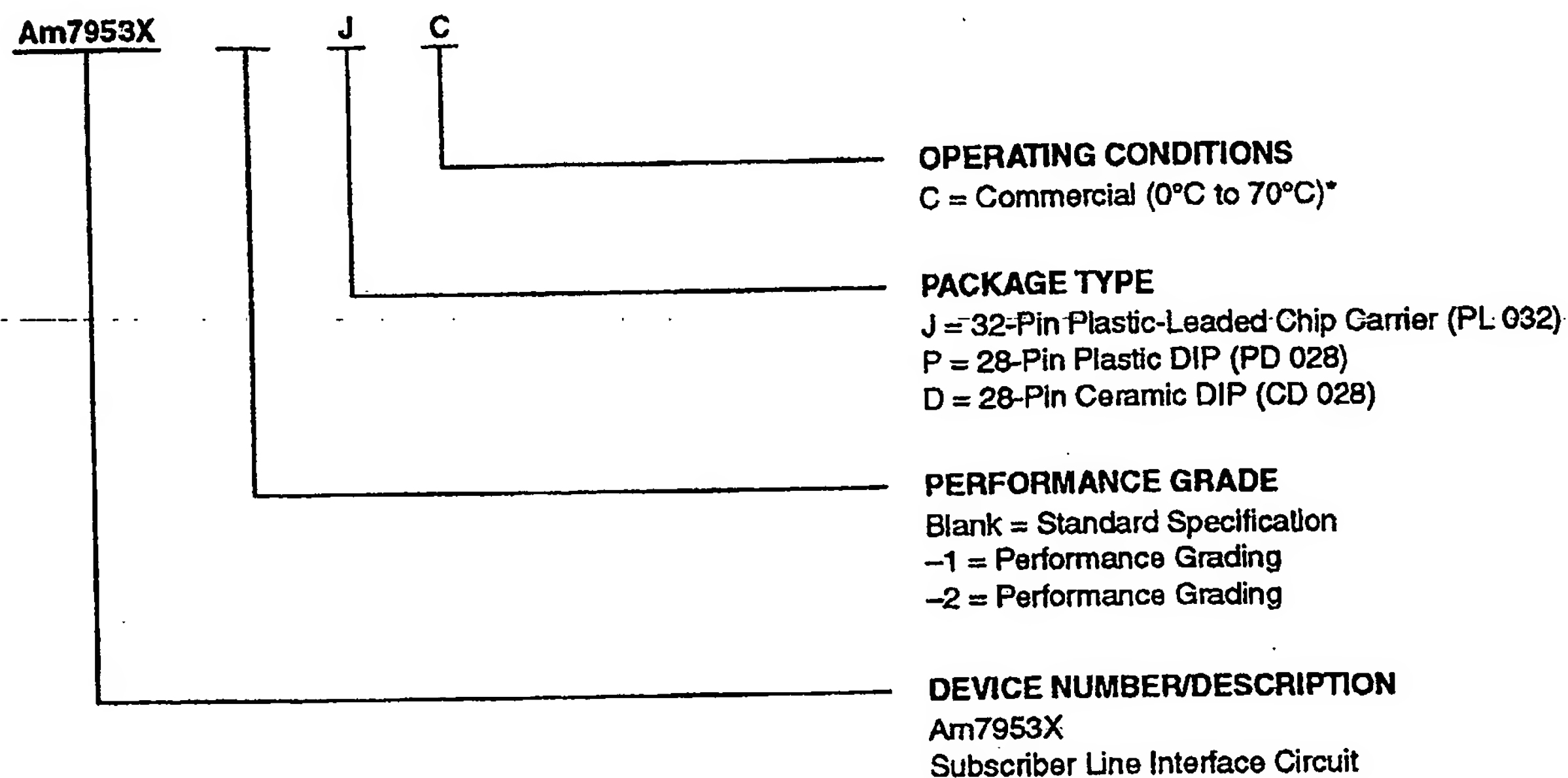
#### Notes:

1. Am79530—E0 and E1 inputs; ring relay sourced internally to BGND; no test relay driver.
2. Am79531—E0 and E1 inputs; ring relay sourced internally to BGND; no test relay driver; ground-key filter pin.
3. Am79534—E0 and E1 inputs; ring and test relay drivers sourced internally to BGND.
4. Am79535—E0 and E1 inputs; ring relay driver sourced internally to BGND; ground-key filter pin.
5. Current gain ( $K_1$ ) = 1000 for all parts.

## ORDERING INFORMATION

### Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of the elements below.



Valid Combinations		
Am7953X		DC
	-1	JC
	-2	PC

#### Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

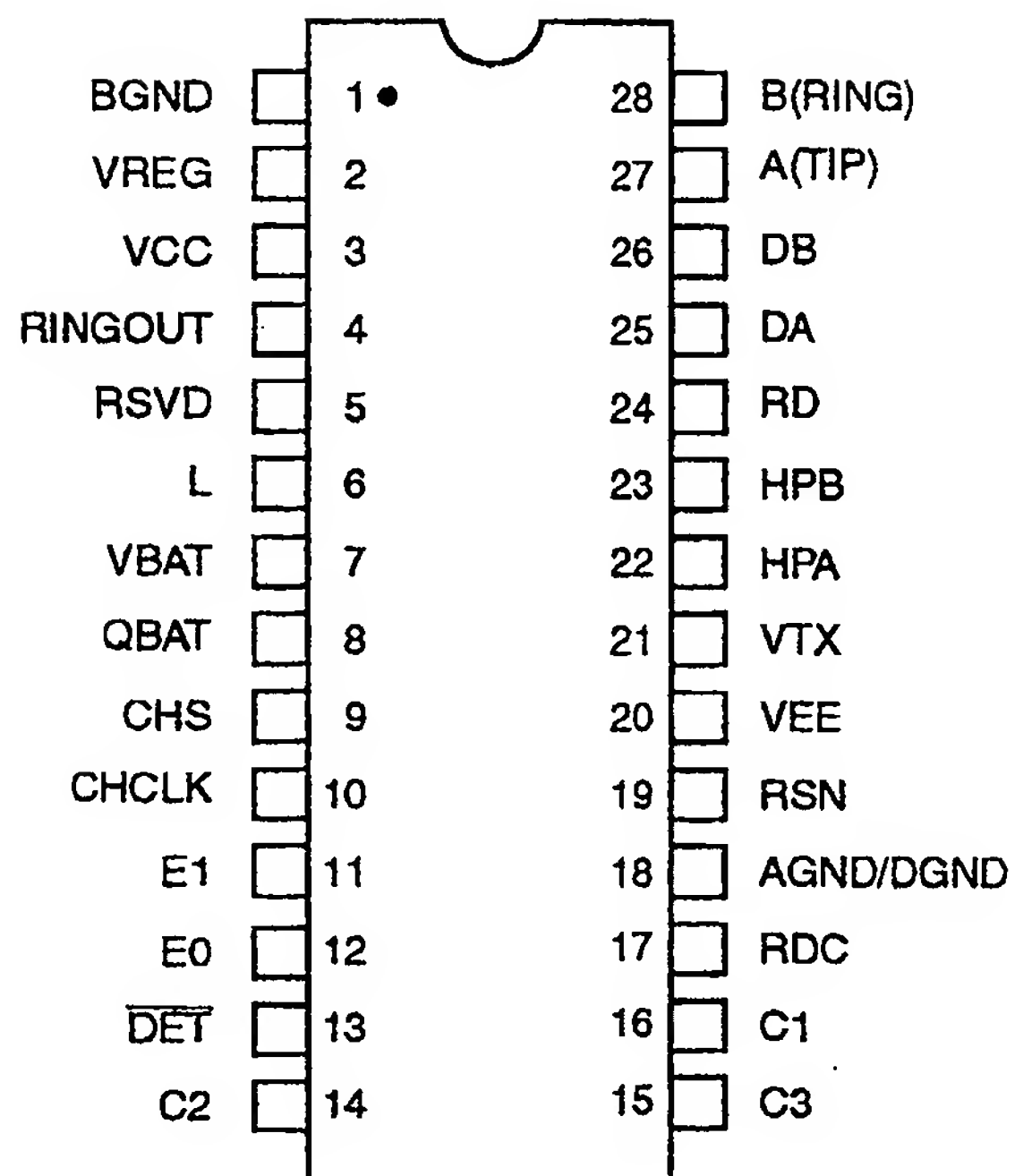
#### Note:

\* Functionality of the device from 0°C to +70°C is guaranteed by production testing. Performance from -40°C to +85°C is guaranteed by characterization and periodic sampling of production units.

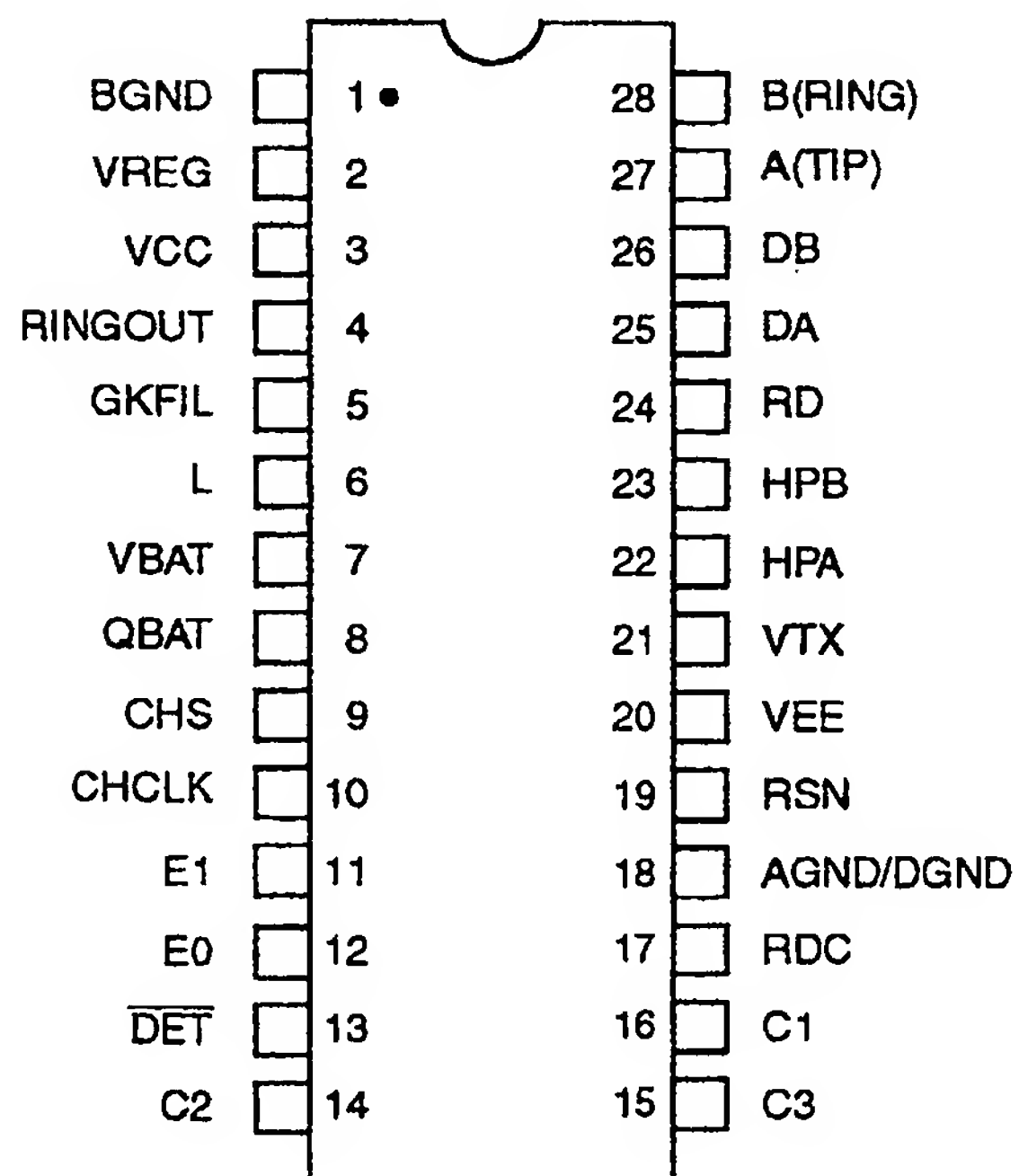
## CONNECTION DIAGRAMS

## Top View

Am79530



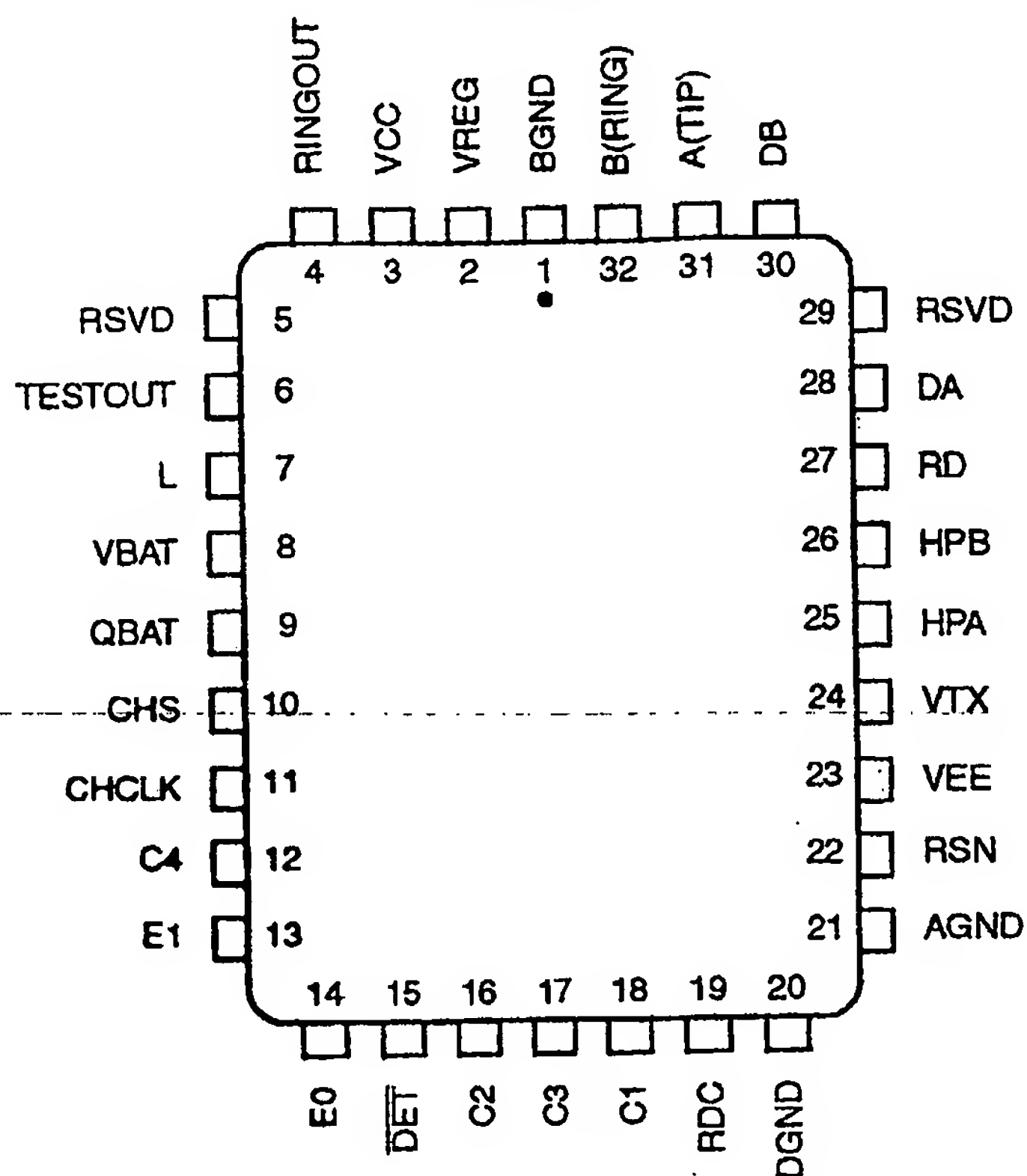
Am79531

**Notes:**

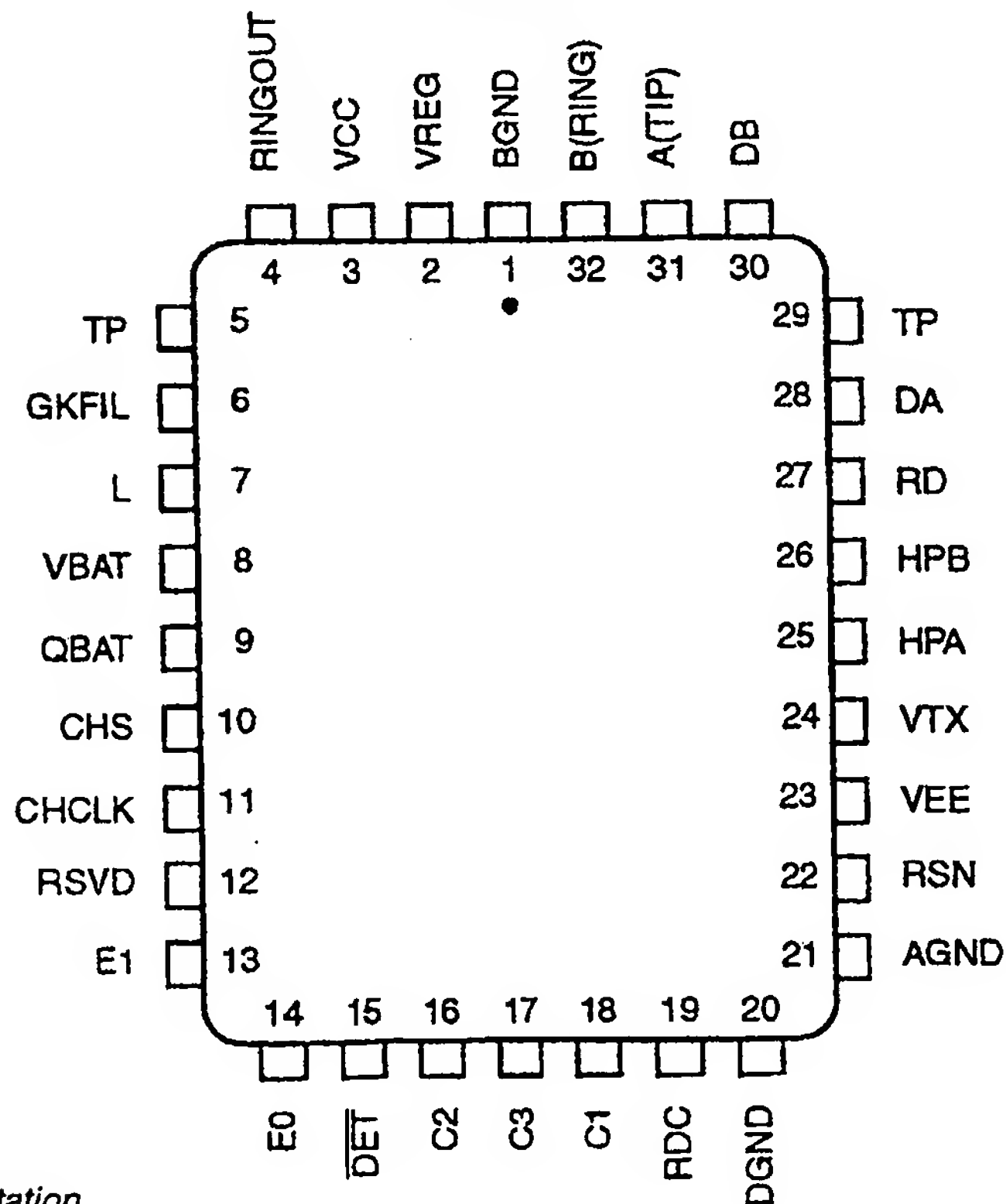
1. Pin 1 is marked for orientation.
2. RSVD = Reserved. Do not connect to this pin.

CONNECTION DIAGRAMS (continued)

Am79534



Am79535



Notes:

1. Pin 1 is marked for orientation.
2. TP is a thermal conduction pin tied to substrate (QBAT).
3. RSVD = Reserved. Do not connect to these pins.

## PIN DESCRIPTIONS

Pin Names	Type	Description
AGND	Gnd	(Am79534 and Am79535) Analog (quiet) ground
AGND/DGND	Gnd	(Am79530 and Am79531) Analog and Digital ground connected internally to a single pin.
A(TIP)	Output	Output of A(TIP) power amplifier.
BGND	Gnd	Battery (power) ground.
B(RING)	Output	Output of B(RING) power amplifier.
C3–C1	Inputs	Decoder. TTL compatible. C3 is MSB and C1 is LSB.
C4	Input	TTL compatible. A logic High enables the driver.
CHCLK	Input	Input to switching regulator (TTL compatible) Frequency = 256 kHz (nominal).
CHS	Input	Chopper Stabilization. Connection for external stabilization components.
DA	Input	Ring-trip negative. Negative input to ring-trip comparator.
DB	Input	Ring-trip positive. Positive input to ring-trip comparator.
DET	Output	Detector. Logic Low indicates that the selected detector is tripped. Logic inputs C3–C1, E0, and E1 select the detector. Open-collector with a built-in 15 k $\Omega$ pull-up resistor.
DGND	Gnd	(Am79534 and Am79535) Digital ground.
E0	Input	Read enable. A logic High enables DET. A logic Low disables DET.
E1	Input	E1 = High connects the ground-key detector to DET, and E1 = Low connects the off-hook or ring-trip detector to DET.
GKFIL	Capacitor	(Am79531 and Am79535) Ground-key filter capacitor. An external capacitor for filtering out high-frequency noise from the ground-key loop can be connected to this pin. An internal 36 k $\Omega$ , $-20\%$ , $+40\%$ resistor is provided to form an RC filter with the external capacitor. In versions that have a GKFIL pin, 3.3 nF minimum capacitance must be connected from the GKFIL pin to ground.
HPA	Capacitor	High-pass filter capacitor; A(TIP) side of high-pass filter capacitor.
HPB	Capacitor	High-pass filter capacitor; B(RING) side of high-pass filter capacitor.
L	Output	Switching Regulator Power Transistor. Connection point for filter inductor and anode of catch diode. Has up to 60 V pulse waveform; isolated from sensitive circuits. You must keep the diode connections short because of the high currents and high di/dt.
QBAT	Battery	Quiet battery. Filtered battery supply for the signal processing circuits.
RD	Resistor	Detector resistor. Threshold modification/filter point for the off-hook detector.
RDC	Resistor	DC feed resistor. Connection point for the DC feed current programming network, which also connects to the receiver summing node (RSN). $V_{RDC}$ is negative for normal polarity and positive for reverse polarity.
RINGOUT	Output	Ring relay driver; sourcing from BGND with internal diode to QBAT.
RSN	Input	The metallic current (AC and DC) between A(TIP) and B(RING) = 1000 x the current into this pin. The networks that program receive gain, two-wire impedance, and feed current all connect to this node. This node is extremely sensitive. Route the 256-kHz chopper clock and switch lines away from the RSN node.
TESTOUT	Output	Test relay driver. Sourcing from BGND with internal diode to QBAT.
TP	Thermal	Thermal pin. Connection for heat dissipation. Internally connected to substrate (QBAT). Leave as open circuit or connected to QBAT. In both cases, the TP pins can connect to an area of copper on the board to enhance heat dissipation
VBAT	Battery	Battery supply through an external protection diode.
VCC	Power	+5 V power supply.
VEE	Power	–5 V power supply.
VREG	Input	Regulated voltage. Provides negative power supply for power amplifiers, connection point for inductor, filter capacitor, and chopper stabilization.
VTX	Output	Transmit Audio; Unity gain version of the A(TIP) and B(RING) metallic voltage. VTX also sources the two-wire input impedance programming network.

**ABSOLUTE MAXIMUM RATINGS**Storage temperature . . . . .  $-55^{\circ}\text{C}$  to  $+150^{\circ}\text{C}$  $V_{\text{CC}}$  with respect to AGND/DGND . . .  $-0.4\text{ V}$  to  $+7.0\text{ V}$  $V_{\text{EE}}$  with respect to AGND/DGND . . .  $+0.4\text{ V}$  to  $-7.0\text{ V}$  $V_{\text{BAT}}$  with respect to AGND/DGND . . .  $+0.4\text{ V}$  to  $-70\text{ V}$ *Note: Rise time of  $V_{\text{BAT}}$  ( $dv/dt$ ) must be limited to  $27\text{ V}/\mu\text{s}$  or less when  $Q_{\text{BAT}}$  bypass =  $0.33\text{ }\mu\text{F}$ .*

BGND with respect to

AGND/DGND . . . . .  $+1.0\text{ V}$  to  $-3.0\text{ V}$ 

A(TIP) or B(RING) to BGND:

Continuous . . . . .  $-70\text{ V}$  to  $+1.0\text{ V}$ 10 ms ( $f = 0.1\text{ Hz}$ ) . . . . .  $-70\text{ V}$  to  $+5.0\text{ V}$ 1  $\mu\text{s}$  ( $f = 0.1\text{ Hz}$ ) . . . . .  $-90\text{ V}$  to  $+10\text{ V}$ 250 ns ( $f = 0.1\text{ Hz}$ ) . . . . .  $-120\text{ V}$  to  $+15\text{ V}$ Current from A(TIP) or B(RING) . . . . .  $\pm 150\text{ mA}$ Voltage on RINGOUT . . . BGND to  $70\text{ V}$  above  $Q_{\text{BAT}}$ Voltage on TESTOUT . . . BGND to  $70\text{ V}$  above  $Q_{\text{BAT}}$ Current through relay drivers . . . . .  $60\text{ mA}$ Voltage on ring-trip inputs (DA and DB) . . .  $V_{\text{BAT}}$  to  $0\text{ V}$ Current into ring-trip inputs . . . . .  $\pm 10\text{ mA}$ Peak current into regulator switch (L pin) . . .  $150\text{ mA}$ Switcher transient peak off voltage on L pin . .  $+1.0\text{ V}$ 

C4-C1, E1, CHCLK to

AGND/DGND . . . . .  $-0.4\text{ V}$  to  $(V_{\text{CC}} + 0.4\text{ V})$ Maximum power dissipation (see note) . . .  $T_{\text{A}} = 70^{\circ}\text{C}$ In 28-pin ceramic DIP package . . . . .  $2.58\text{ W}$ In 28-pin plastic DIP package . . . . .  $1.4\text{ W}$ In 32-pin PLCC package . . . . .  $1.74\text{ W}$ *Note: Thermal limiting circuitry on chip will shut down the circuit at a junction temperature of about  $165^{\circ}\text{C}$ . The device should never be exposed to this temperature. Operation above  $145^{\circ}\text{C}$  junction temperature may degrade device reliability. See the SLIC Packaging Considerations for more information.**Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability.***OPERATING RANGES****Commercial (C) Devices**Ambient temperature . . . . .  $0^{\circ}\text{C}$  to  $+70^{\circ}\text{C}^*$  $V_{\text{CC}}$  . . . . .  $4.75\text{ V}$  to  $5.25\text{ V}$  $V_{\text{EE}}$  . . . . .  $-4.75\text{ V}$  to  $-5.25\text{ V}$  $V_{\text{BAT}}$  . . . . .  $-40\text{ V}$  to  $-58\text{ V}$ AGND/DGND . . . . .  $0\text{ V}$ 

BGND with respect to

AGND/DGND . . . . .  $-100\text{ mV}$  to  $+100\text{ mV}$ Load resistance on VTX to ground . . . . .  $10\text{ k}\Omega$  min*Operating Ranges define those limits between which the functionality of the device is guaranteed.**\* Functionality of the device from  $0^{\circ}\text{C}$  to  $+70^{\circ}\text{C}$  is guaranteed by production testing. Performance from  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$  is guaranteed by characterization and periodic sampling of production units.*



## ELECTRICAL CHARACTERISTICS

Description	Test Conditions (See Note 1)	Min	Typ	Max	Unit	Note
Analog ( $V_{TX}$ ) output impedance			3		$\Omega$	4
Analog ( $V_{TX}$ ) output offset	0°C to +70°C -1*	-35 -30		+35 +30	mV	4 4
	-40°C to +85°C -1	-40 -35		+40 +35		
Analog (RSN) input impedance	300 Hz to 3.4 kHz		1	20	$\Omega$	4
Longitudinal impedance at A or B				35		
Overload level $Z_{2WIN} = 600 \Omega$ to $900 \Omega$	4-wire 2-wire	-3.1		+3.1	Vpk	2
<b>Transmission Performance, 2-Wire Impedance</b>						
2-wire return loss (See Test Circuit D)	300 Hz to 500 Hz 500 Hz to 2.5 kHz 2.5 kHz to 3.4 kHz	26 26 20			dB	4, 10
<b>Longitudinal Balance (2-Wire and 4-Wire, See Test Circuit C)</b>						
$R_L = 600 \Omega$ Longitudinal to metallic L-T, L-4	300 Hz to 3.4 kHz -1*	48 52			dB	4
Longitudinal to metallic L-T, L-4	200 Hz to 1 kHz: Normal polarity 0°C to +70°C -2*	63				
	Normal polarity -40°C to +85°C -2	58				
	Reverse polarity -2	54				
	1 kHz to 3.4 kHz: Normal polarity 0°C to +70°C -2*	58				
	Normal polarity -40°C to +85°C -2	54				
	Reverse polarity -2	54				
Longitudinal signal generation 4-L	300 Hz to 800 Hz 300 Hz to 800 Hz -1*	40 42				
Longitudinal current capability per wire	Active state OHT state		25 18		mArms	4
<b>Insertion Loss (2- to 4-Wire and 4- to 2-Wire, See Test Circuits A and B)</b>						
Gain accuracy	0 dBm, 1 kHz 0°C to +70°C	-0.15		+0.15	dB	4
	0 dBm, 1 kHz -40°C to +85°C	-0.20		+0.20		
	0 dBm, 1 kHz 0°C to +70°C -1*	-0.1		+0.1		
	0 dBm, 1 kHz -40°C to +85°C -1	-0.15		+0.15		
Variation with frequency	300 Hz to 3.4 kHz (relative to 1 kHz): 0°C to +70°C	-0.1		+0.1		4
	-40°C to +85°C	-0.15		+0.15		
Gain tracking	+7 dBm to -55 dBm: 0°C to +70°C -40°C to +85°C	-0.1 -0.15		+0.1 +0.15		4

**Note:**

\* P.G. = Performance Grade (-2 performance parameters are equivalent to -1 performance parameters, except where indicated).

**ELECTRICAL CHARACTERISTICS (continued)**

Description	Test Conditions (See Note 1)	Min	Typ	Max	Unit	Note
Balance Return Signal (4- to 4-Wire, See Test Circuit B)						
Gain accuracy	0 dBm, 1 kHz 0°C to +70°C	-0.15		+0.15	dB	4
	0 dBm, 1 kHz -40°C to +85°C	-0.20		+0.20		
	0 dBm, 1 kHz 0°C to +70°C	-1* -0.1		+0.1		4
	0 dBm, 1 kHz -40°C to +85°C	-1 -0.15		+0.15		
Variation with frequency	300 Hz to 3.4 kHz (relative to 1 kHz): 0°C to +70°C -40°C to +85°C	-0.1 -0.15		+0.1 +0.15		4
Gain tracking	+7 dBm to -55 dBm: 0°C to +70°C	-0.1		+0.1		4
	-40°C to +85°C	-0.15		+0.15		4
Group delay	f = 1 kHz		5.3		μs	4
Total Harmonic Distortion (2- to 4-Wire or 4- to 2-Wire, See Test Circuits A and B)						
Total harmonic distortion	0 dBm, 300 Hz to 3.4 kHz +9 dBm, 300 Hz to 3.4 kHz		-64 -55	-50 -40	dB	
Idle Channel Noise						
C-message weighted noise	2-wire: 0°C to +70°C		+7	+15	dBmC	4
	2-wire: 0°C to +70°C	-1*	+7	+12		
	2-wire: -40°C to +85°C		+7	+15		4
	4-wire 0°C to +70°C		+7	+15		
Psophometric weighted noise	4-wire 0°C to +70°C	-1*	+7	+12	dBmp	7
	4-wire 0°C to +70°C		+7	+12		
	4-wire -40°C to +85°C		+7	+15		4
	2-wire 0°C to +70°C		-83	-75		7
	2-wire 0°C to +70°C	-1*	-83	-78		
	2-wire -40°C to +85°C		-83	-75		4
Single Frequency Out-of-Band Noise (See Test Circuit E)						
Metallic	4 kHz to 9 kHz		-76		dBm	4, 5, 9
	9 kHz to 1 MHz		-76			4, 5, 9
	256 kHz and harmonics		-57			4, 5
Longitudinal	1 kHz to 15 kHz		-70		dBm	4
	Above 15 kHz		-85			4, 5, 9
	256 kHz and harmonics		-57			4, 5
DC Feed Currents (See Figure 1) BAT = -48 V						
Active state loop-current accuracy	I <sub>LOOP</sub> (nominal) = 40 mA	-7.5		+7.5	%	
OHT state	R <sub>L</sub> = 600 Ω	18	20	22	mA	
Tip Open state	R <sub>L</sub> = 600 Ω			1.0		
Open Circuit state	R <sub>L</sub> = 0 Ω			1.0		
Fault current limit, I <sub>L</sub> LIM (I <sub>AX</sub> + I <sub>BX</sub> )	A and B shorted to GND			130		



## ELECTRICAL CHARACTERISTICS (continued)

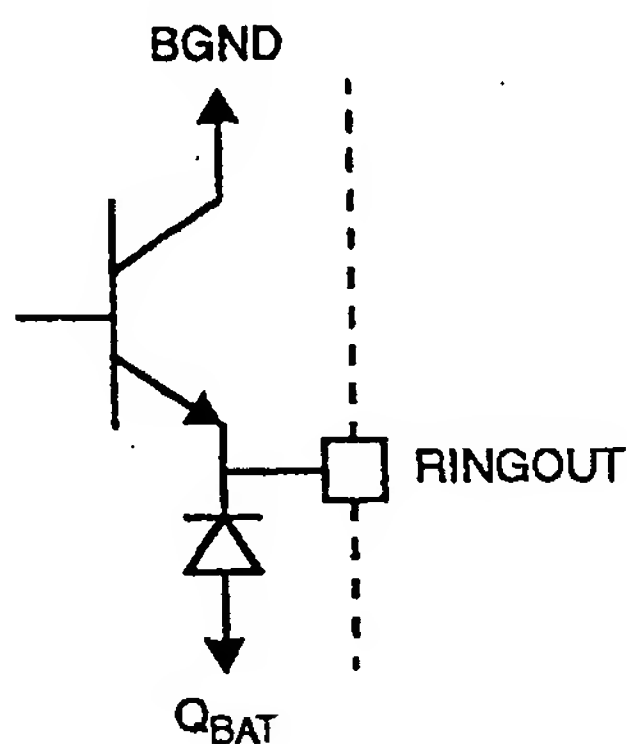
Description	Test Conditions (See Note 1)	Min	Typ	Max	Unit	Note
Power Dissipation BAT = -48 V, Normal Polarity						
On-hook Open Circuit state	-1*		35 35	120 80	mW	
On-hook OHT state	-1*		135 135	250 200		
On-hook Active state	-1*		200 200	400 300		
Off-hook OHT state	R <sub>L</sub> = 600 Ω		500	750		
Off-hook Active state	R <sub>L</sub> = 600 Ω		650	1000		
Supply Currents						
V <sub>CC</sub> on-hook supply current	Open Circuit state OHT state Active state		3.0 6.0 7.5	4.5 10.0 12.0	mA	
V <sub>EE</sub> on-hook supply current	Open Circuit state OHT state Active state		1.0 2.2 2.7	2.3 3.5 6.0		
V <sub>BAT</sub> on-hook supply current	Open Circuit state OHT state Active state		0.4 3.0 4.0	1.0 5.0 6.0		
Power Supply Rejection Ratio (V <sub>RI</sub> PPLE = 50 mVrms)						
V <sub>CC</sub>	50 Hz to 3.4 kHz	-1*	25 30	45 45	dB	6, 7
	3.4 kHz to 50 kHz	-1	22 25	35 35		
V <sub>EE</sub>	50 Hz to 3.4 kHz	-1*	20 25	40 40		
	3.4 kHz to 50 kHz	-1	10 10	25 25		
V <sub>BAT</sub>	50 Hz to 3.4 kHz	-1*	27 30	45 45		
	3.4 kHz to 50 kHz	-1	20 25	40 40		
Off-Hook Detector						
Current threshold accuracy	I <sub>DET</sub> = 365/R <sub>D</sub> nominal	-20		+20	%	
Ground-Key Detector Thresholds, Active State, BAT = -48 V (See Test Circuit F)						
Ground-key resistance threshold	B(RING) to GND	2.0	5.0	10.0	kΩ	
Ground-key current threshold	B(RING) to GND Midpoint to GND		9		mA	8
Ring-Trip Detector Input						
Bias current		-5	-0.05		μA	
Offset voltage	Source resistance 0 to 2 MΩ	-50	0	+50	mV	11

# ELECTRICAL CHARACTERISTICS (continued)

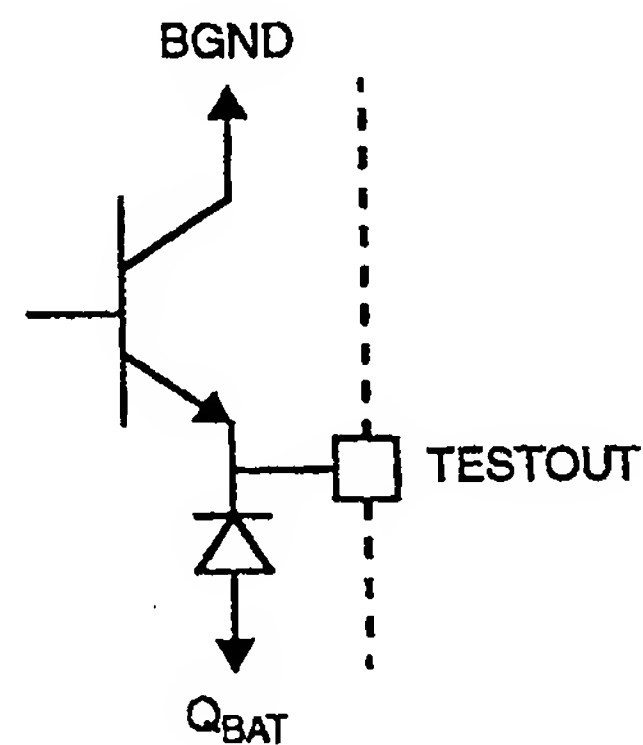
Description	Test Conditions (See Note 1)	Min	Typ	Max	Unit	Note
Logic Inputs (C4–C1, E0, E1, and CHCLK)						
Input High voltage		2.0			V	
Input Low voltage				0.8		
Input High current	All inputs except E1 Input E1	–75 –75		40 45	μA	
Input Low current		–0.4			mA	
Logic Output ( $\overline{DET}$ )						
Output Low voltage	$I_{OUT} = 0.8\text{ mA}$			0.4	V	
Output High voltage	$I_{OUT} = -0.1\text{ mA}$	2.4				
Relay Driver Outputs (RINGOUT, TESTOUT)						
On voltage	50 mA source	BGND – 2	BGND – 0.95		V	
Off leakage			0.5	100	μA	
Clamp voltage	50 mA sink	$Q_{BAT} - 2$			V	

## RELAY DRIVER SCHEMATICS

Am79530/Am79531/  
Am79534/Am79535



Am79534



16854C-03

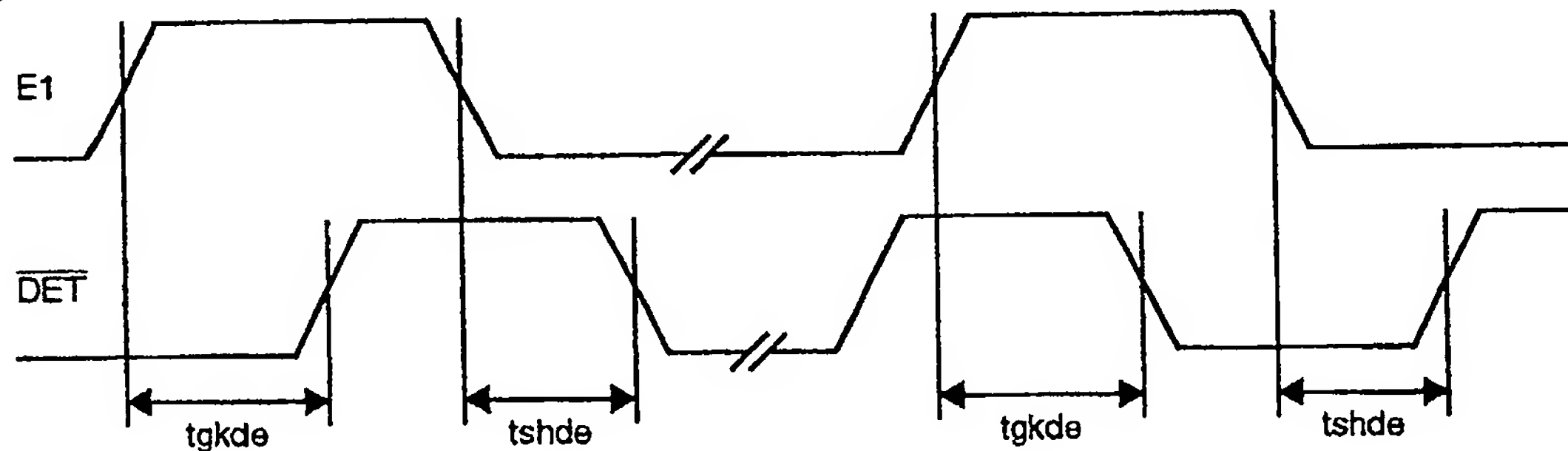
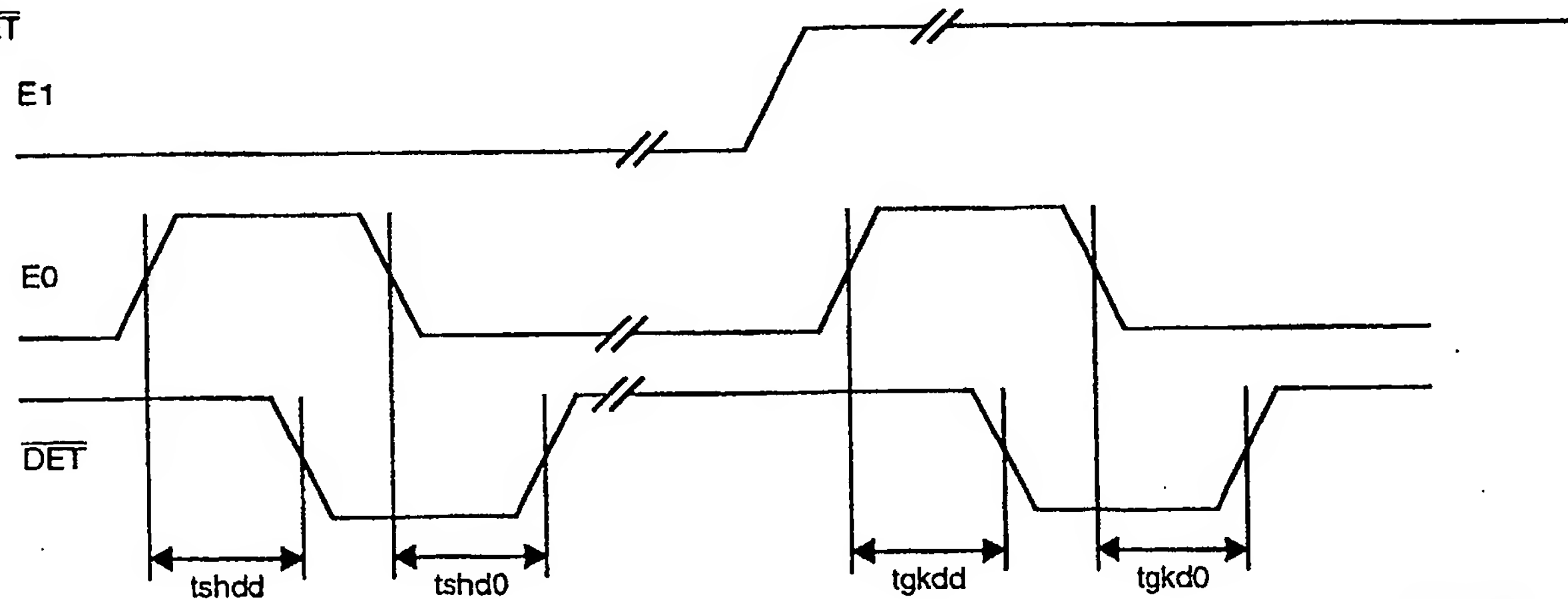
## SWITCHING CHARACTERISTICS

Am79530/Am79531/Am79534/Am79535

Symbol	Parameter	Test Conditions	Temperature Range	Min	Typ	Max	Unit	Note
tgkde	E1 Low to $\overline{\text{DET}}$ High (E0 = 1)	Ground-key Detect state $R_L$ open, $R_G$ connected (See Figure H)	0°C to +70°C -40°C to +85°C			3.8 4.0	$\mu\text{s}$	4
	E1 Low to $\overline{\text{DET}}$ Low (E0 = 1)		0°C to +70°C -40°C to +85°C			1.1 1.6		
tgkdd	E0 High to $\overline{\text{DET}}$ Low (E1 = 0)		0°C to +70°C -40°C to +85°C			1.1 1.6		
tgkd0	E0 Low to $\overline{\text{DET}}$ High (E1 = 0)		0°C to +70°C -40°C to +85°C			3.8 4.0		
tshde	E1 High to $\overline{\text{DET}}$ Low (E0 = 1)	Switchhook Detect state $R_L = 600\ \Omega$ , $R_G$ open (See Figure G)	0°C to +70°C -40°C to +85°C			1.2 1.7		
	E1 High to $\overline{\text{DET}}$ High (E0 = 1)		0°C to +70°C -40°C to +85°C			3.8 4.0		
tshdd	E0 High to $\overline{\text{DET}}$ Low (E1 = 1)		0°C to +70°C -40°C to +85°C			1.1 1.6		
tshd0	E0 Low to $\overline{\text{DET}}$ High (E1 = 1)		0°C to +70°C -40°C to +85°C			3.8 4.0		

## SWITCHING WAVEFORMS

Am79530/Am79531/Am79534/Am79535

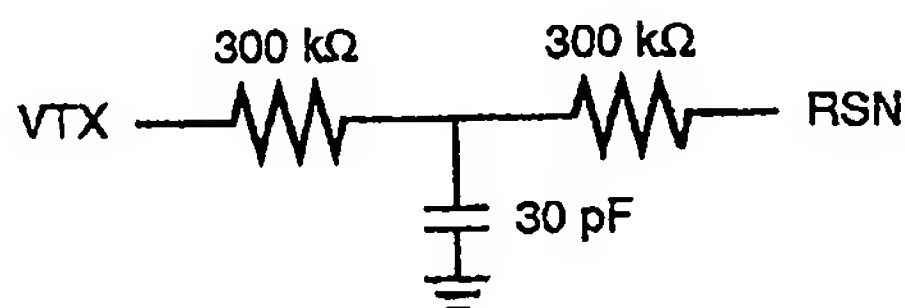
E1 to  $\overline{\text{DET}}$ E0 to  $\overline{\text{DET}}$ **Note:**

All delays measured at 1.4 V level.

16854C-02

**Notes:**

1. Unless otherwise noted, test conditions are  $BAT = -48\text{ V}$ ,  $V_{CC} = +5\text{ V}$ ,  $V_{EE} = -5\text{ V}$ ,  $R_L = 600\ \Omega$ ,  $C_{HP} = 0.22\ \mu\text{F}$ ,  $R_{DC1} = R_{DC2} = 31.25\text{ k}\Omega$ ,  $C_{DC} = 0.1\ \mu\text{F}$ ,  $R_D = 51.1\text{ k}\Omega$ , no fuse resistors, two-wire AC output impedance, programming impedance ( $Z_T$ ) =  $600\text{ k}\Omega$  resistive, receive input summing impedance ( $Z_{RX}$ ) =  $300\text{ k}\Omega$  resistive. (See Table 2 for component formulas.)
2. Overload level is defined when  $THD = 1\%$ .
3. Balance return signal is the signal generated at  $V_{TX}$  by  $V_{RX}$ . This specification assumes the two-wire AC load impedance matches the impedance programmed by  $Z_T$ .
4. Not tested in production. This parameter is guaranteed by characterization or correlation to other tests.
5. These tests are performed with a longitudinal impedance of  $90\ \Omega$  and metallic impedance of  $300\ \Omega$  for frequencies below  $12\text{ kHz}$  and  $135\ \Omega$  for frequencies greater than  $12\text{ kHz}$ . These tests are extremely sensitive to circuit board layout.
6. This parameter is tested at  $1\text{ kHz}$  in production. Performance at other frequencies is guaranteed by characterization.
7. When the SLIC is in the Anti-sat 2 operating region, this parameter is degraded. The exact degradation depends on system design. The Anti-sat 2 region occurs at high loop resistances when  $|V_{BAT} - V_{AX} - V_{BX}|$  is less than approximately  $11\text{ V}$ .
8. "Midpoint" is defined as the connection point between two  $300\ \Omega$  series resistors connected between A(TIP) and B(RING).
9. Fundamental and harmonics from  $256\text{ kHz}$  switch-regulator chopper are not included.
10. Assumes the following  $Z_T$  network:



11. Tested with  $0\ \Omega$  source impedance.  $2\text{ M}\Omega$  is specified for system design purposes only.
12. Group delay can be reduced considerably by using a  $Z_T$  network such as that shown in Note 10 above. The network reduces the group delay to less than  $2\ \mu\text{s}$ . The effect of group delay on linecard performance may be compensated for by using QSLAC™ or DSLAC™ devices.

Table 1. SLIC Decoding

State	C3 C2 C1	Two-Wire Status	DET Output (E0 = 1*)	
			E1 = 0	E1 = 1
0	0 0 0	Open Circuit	Ring trip	Ring trip
1	0 0 1	Ringling	Ring trip	Ring trip
2	0 1 0	Active	Loop detector	Ground key
3	0 1 1	On-hook TX (OHT)	Loop detector	Ground key
4	1 0 0	Tip Open	Loop detector	—
5	1 0 1	Reserved	Loop detector	—
6	1 1 0	Active Polarity Reversal	Loop detector	Ground key
7	1 1 1	OHT Polarity Reversal	Loop detector	Ground key

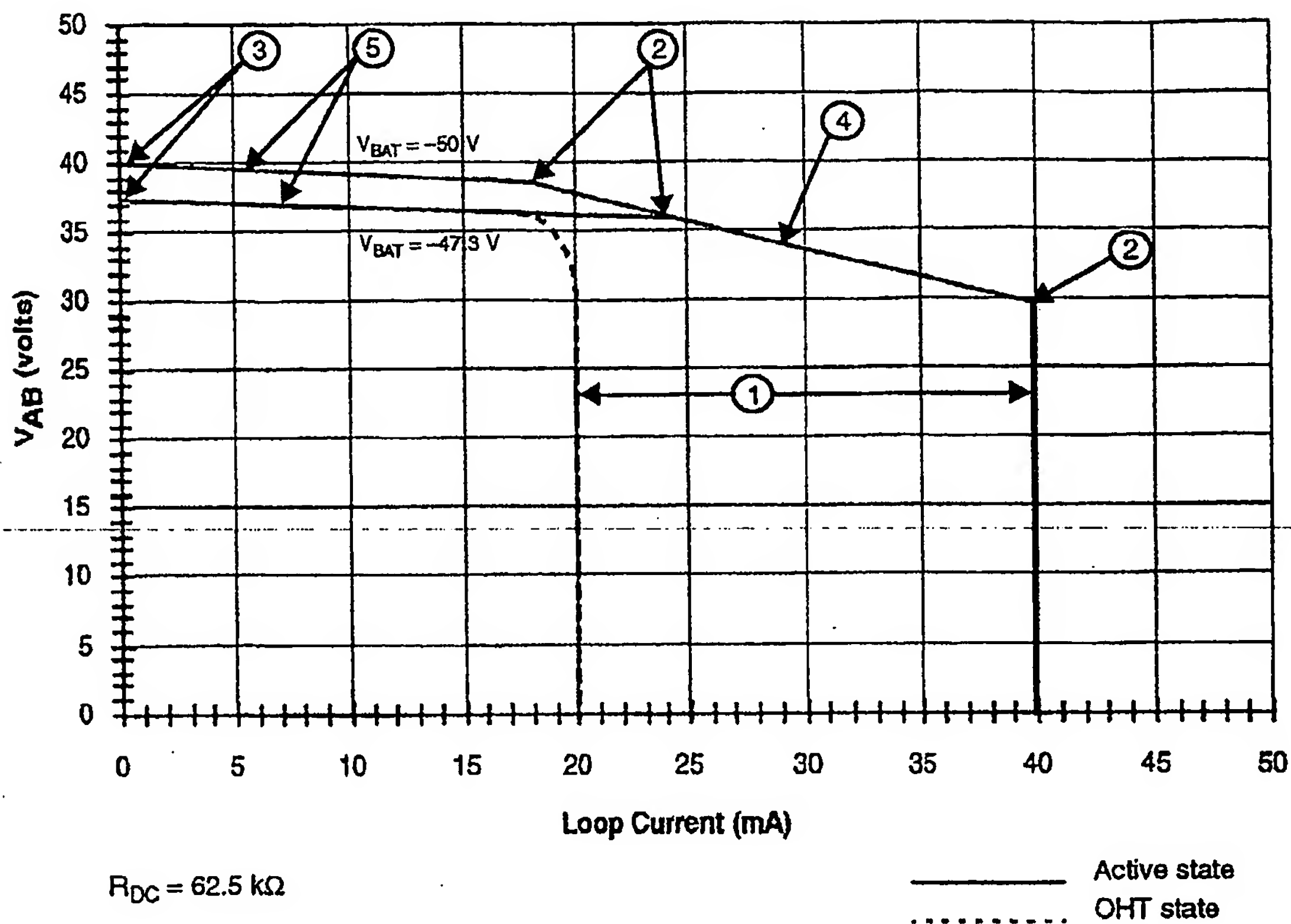
**Note:**

\* For the Am79530, Am79531, Am79534, and Am79535, a logic Low on E0 disables the  $\overline{DET}$  output into the open-collector state.

Table 2. User-Programmable Components

$Z_T = 1000(Z_{2WIN} - 2R_F)$	Where $Z_T$ is connected between the VTX and RSN pins. The fuse resistors are $R_F$ and $Z_{2WIN}$ is the desired 2-wire AC input impedance. When computing $Z_T$ , the internal current amplifier pole and any external stray capacitance between VTX and RSN must be taken into account.
$Z_{RX} = \frac{Z_L}{G_{42L}} \cdot \frac{1000 \cdot Z_T}{Z_T + 1000(Z_L + 2R_F)}$	Where $Z_{RX}$ is connected from $V_{RX}$ to the RSN pin, $Z_T$ is defined above, and $G_{42L}$ is the desired receive gain.
$R_{DC1} + R_{DC2} = \frac{2500}{I_{FBED}}$ $C_{DC} = 1.5 \text{ ms} \cdot \frac{R_{DC1} + R_{DC2}}{R_{DC1} \cdot R_{DC2}}$	Where $R_{DC1}$ , $R_{DC2}$ , and $C_{DC}$ form the network connected to the RDC pin. $R_{DC1}$ and $R_{DC2}$ are approximately equal.
$R_D = \frac{365}{I_T}, \quad C_D = \frac{0.5 \text{ ms}}{R_D}$	Where $R_D$ and $C_D$ form the network connected from RD to -5 V and $I_T$ is the threshold current between on hook and off hook.

# DC FEED CHARACTERISTICS



## Notes:

### 1. Constant-current region:

Active state:  $I_L = \frac{2500}{R_{DC}}$

OHT state:  $I_L = \frac{1}{2} \cdot \frac{2500}{R_{DC}}$

### 2. Anti-sat turn-on (Active state):

Anti-sat -1:  $V_{AB} = 29.95 \text{ V}$

Anti-sat -2:  $V_{AB} = 1.082|V_{BAT}| - 15.149$

### 3. Open Circuit voltage (Active state):

$V_{AB} = 0.9|V_{BAT}| - 4.995, \quad |V_{BAT}| < 56.9 \text{ V}$

$V_{AB} = 46.25 \text{ V}, \quad |V_{BAT}| \geq 56.9 \text{ V}$

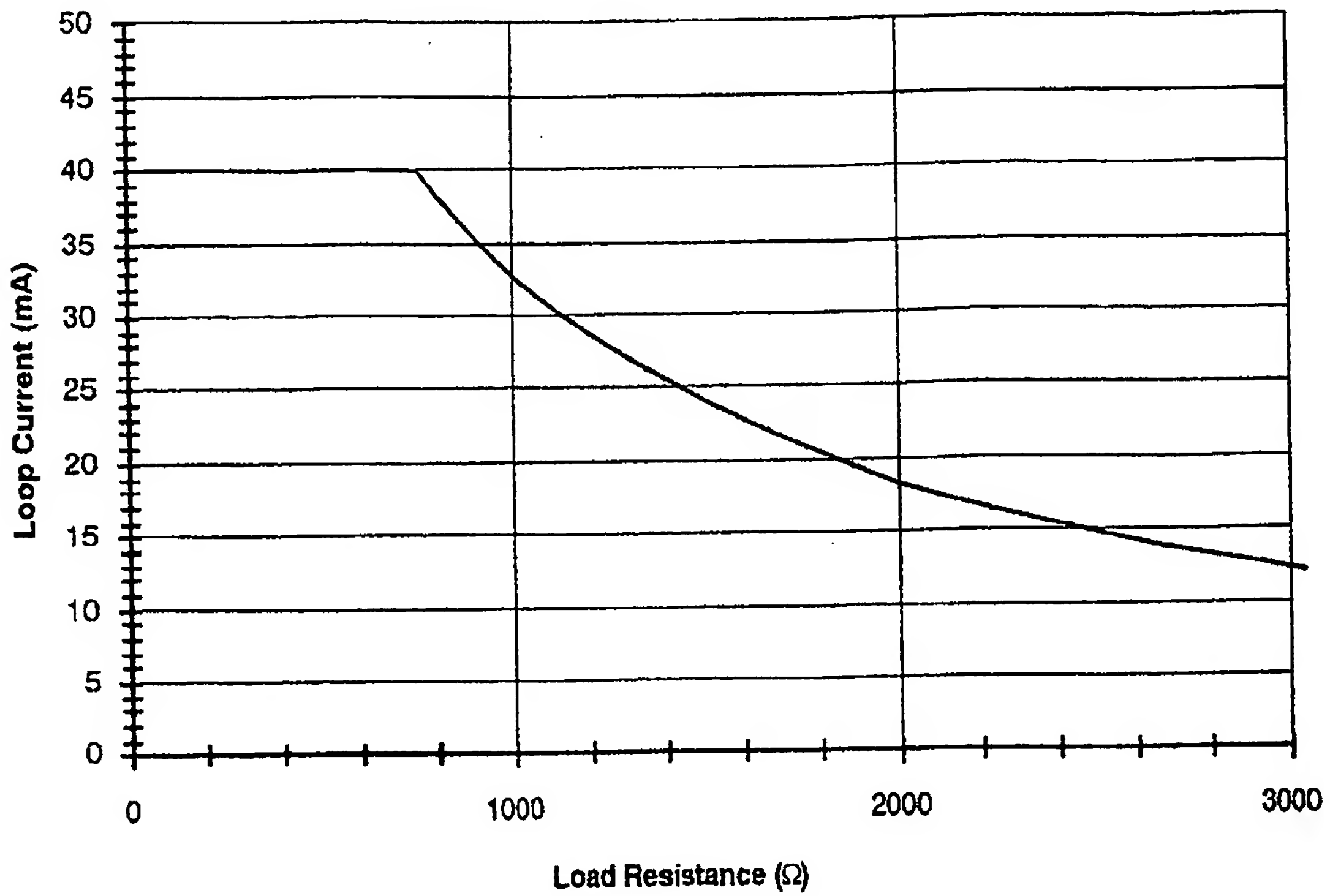
4. Anti-sat -1 region:  $V_{AB} = 46.25 - I_L \frac{R_{DC}}{150.6}$

5. Anti-sat -2 region:  $V_{AB} = 0.9|V_{BAT}| - 4.995 - I_L \frac{R_{DC}}{1128}$

a. V<sub>A</sub>-V<sub>B</sub> (V<sub>AB</sub>) Voltage vs. Loop Current (Typical)



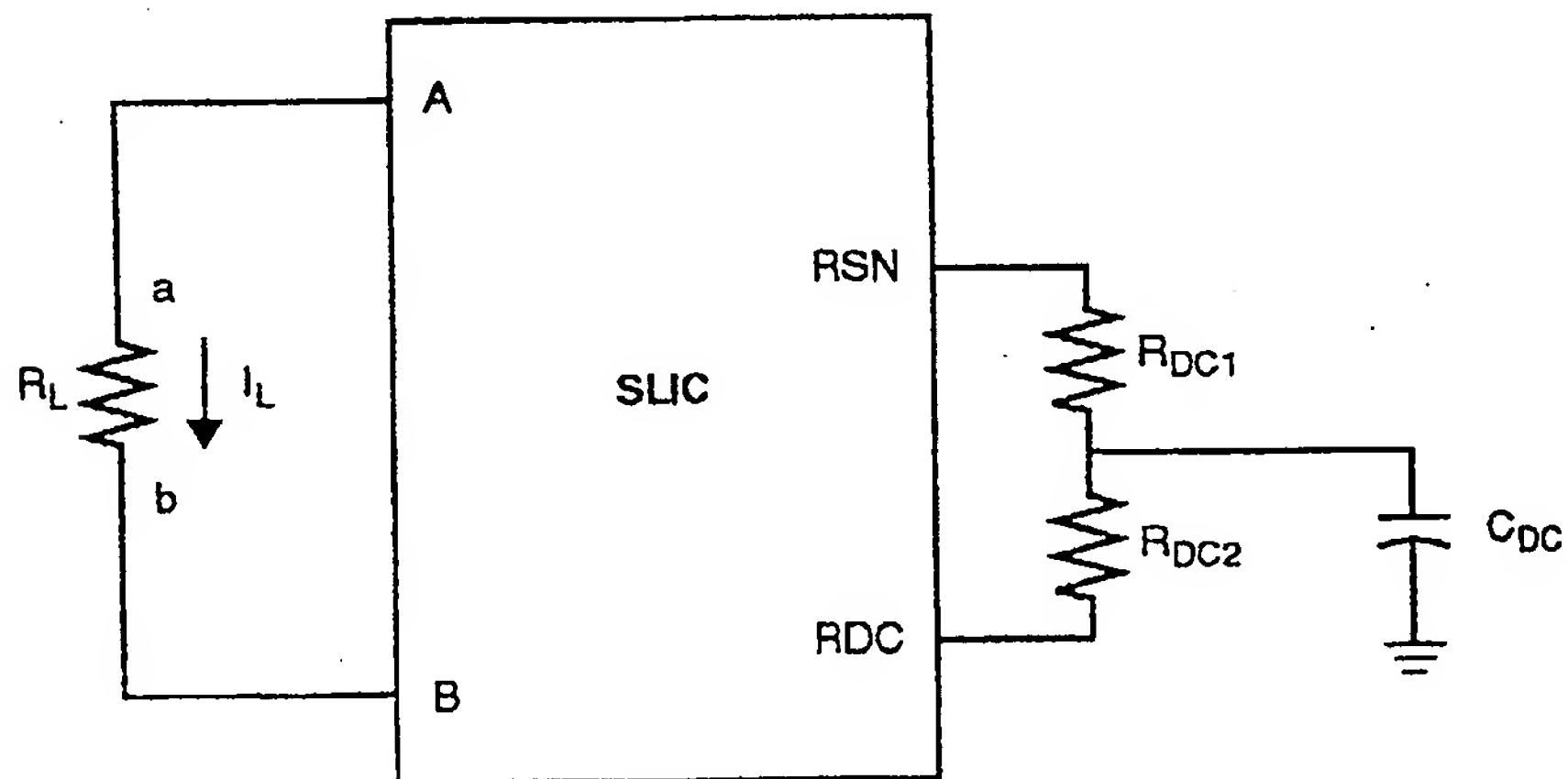
# DC FEED CHARACTERISTICS (continued)



$$R_{DC} = 62.5 \text{ k}\Omega$$

$$V_{BAT} = -47.3 \text{ V}$$

b. Loop Current vs. Load Resistance (Typical)

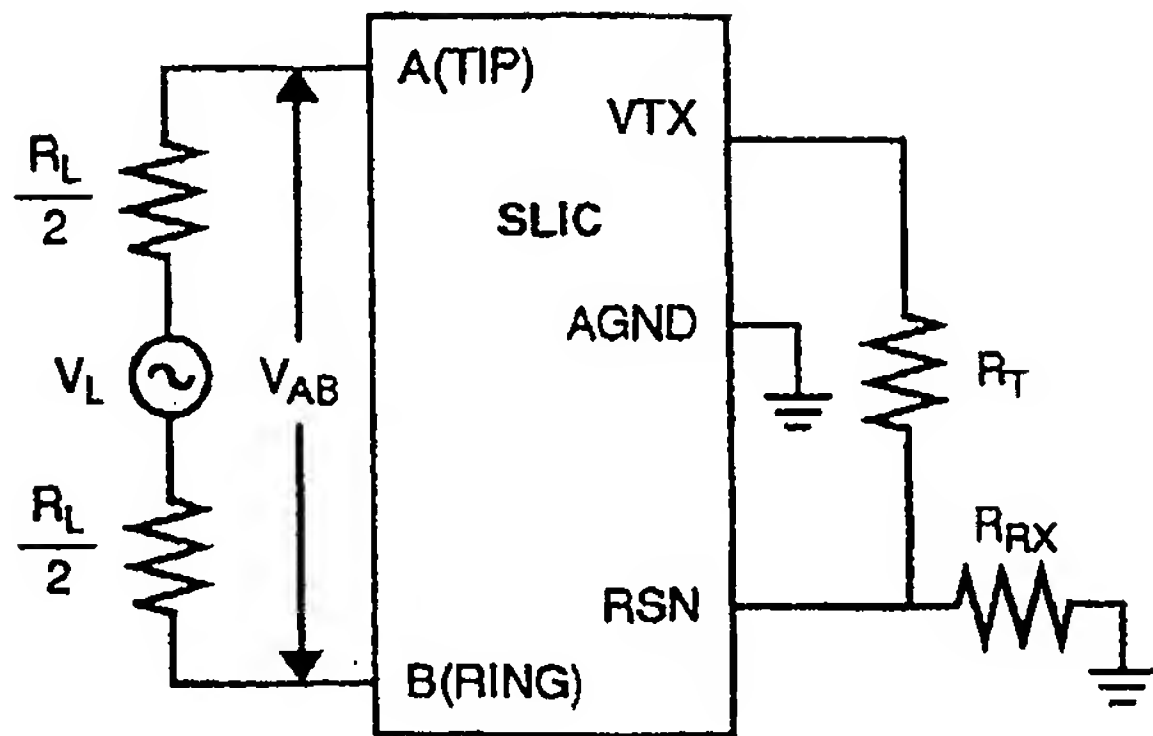


Feed current programmed by  $R_{DC1}$  and  $R_{DC2}$

c. Feed Programming

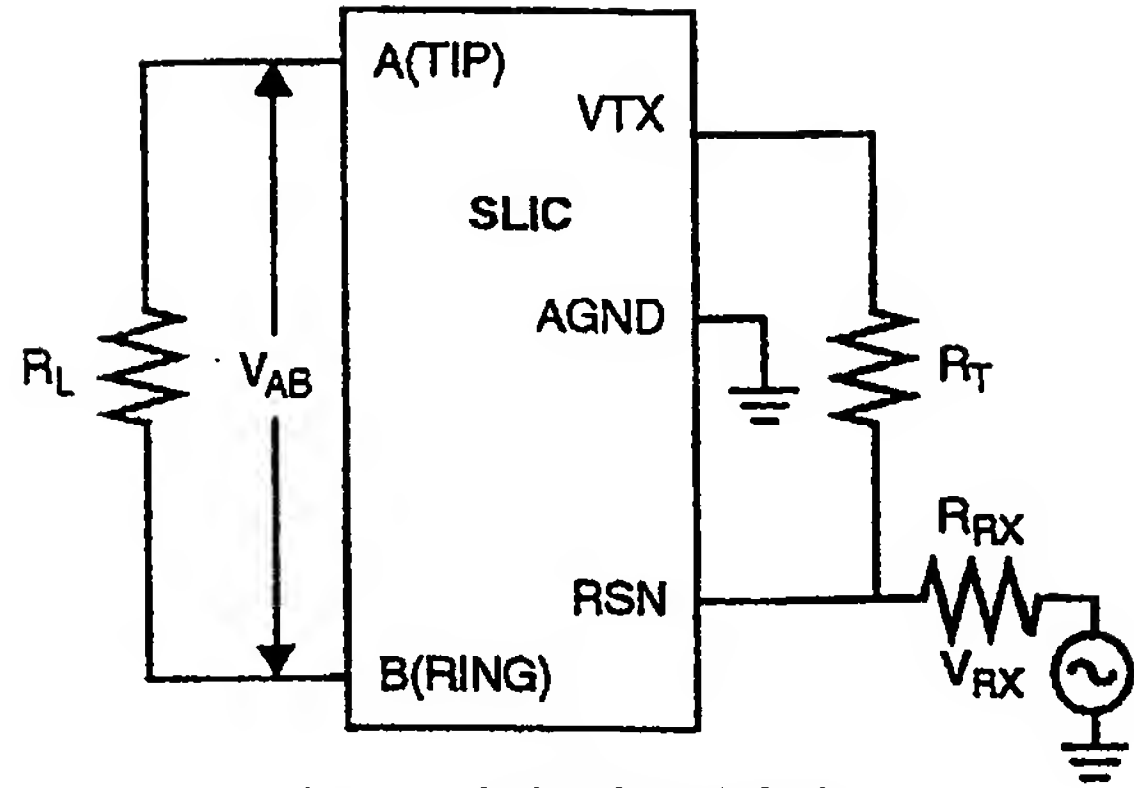
Figure 1. DC Feed Characteristics

# TEST CIRCUITS



$$I_{L2-4} = -20 \log (V_{TX} / V_{AB})$$

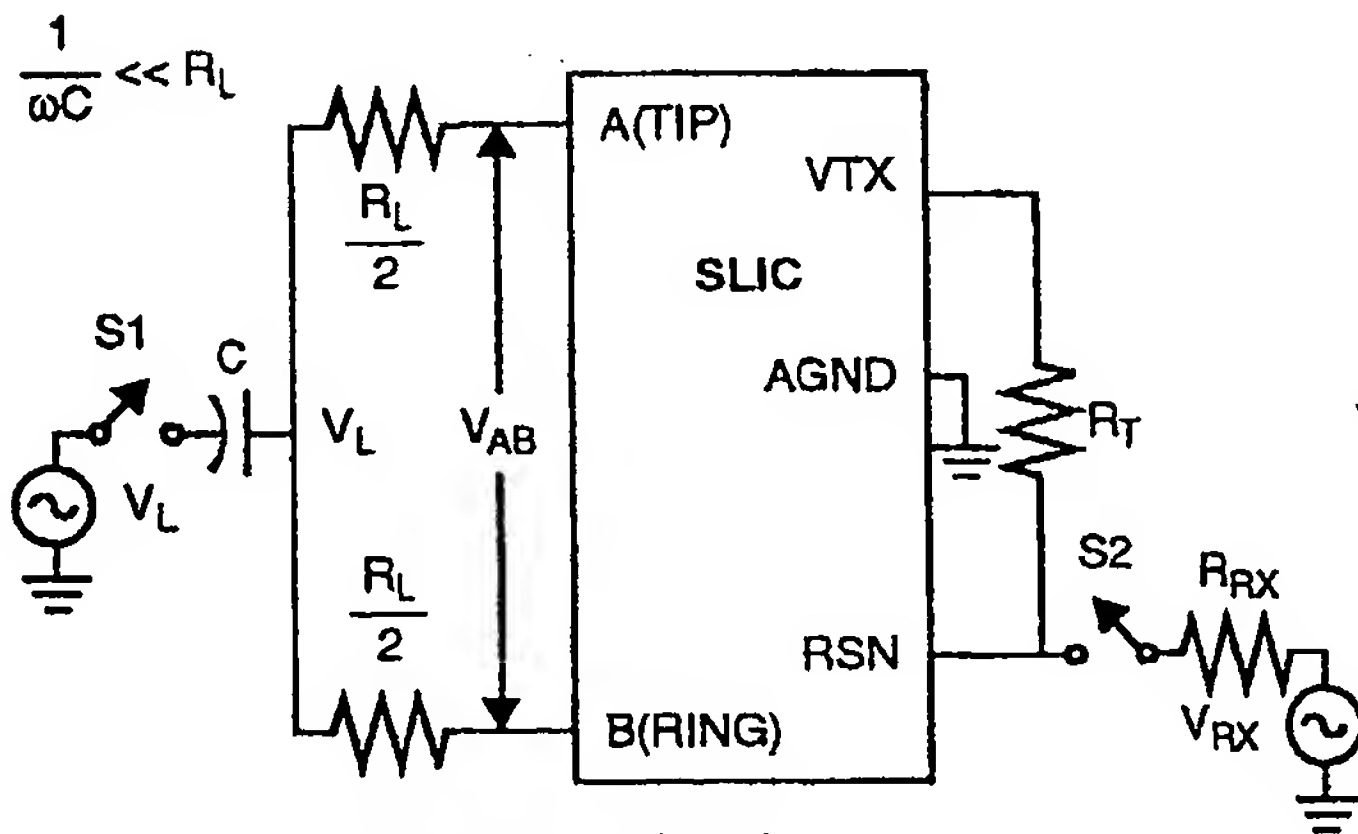
A. Two- to Four-Wire Insertion Loss



$$I_{L4-2} = -20 \log (V_{AB} / V_{RX})$$

$$BRS = 20 \log (V_{TX} / V_{RX})$$

B. Four- to Two-Wire Insertion Loss and Balance Return Signal



S2 Open, S1 Closed:

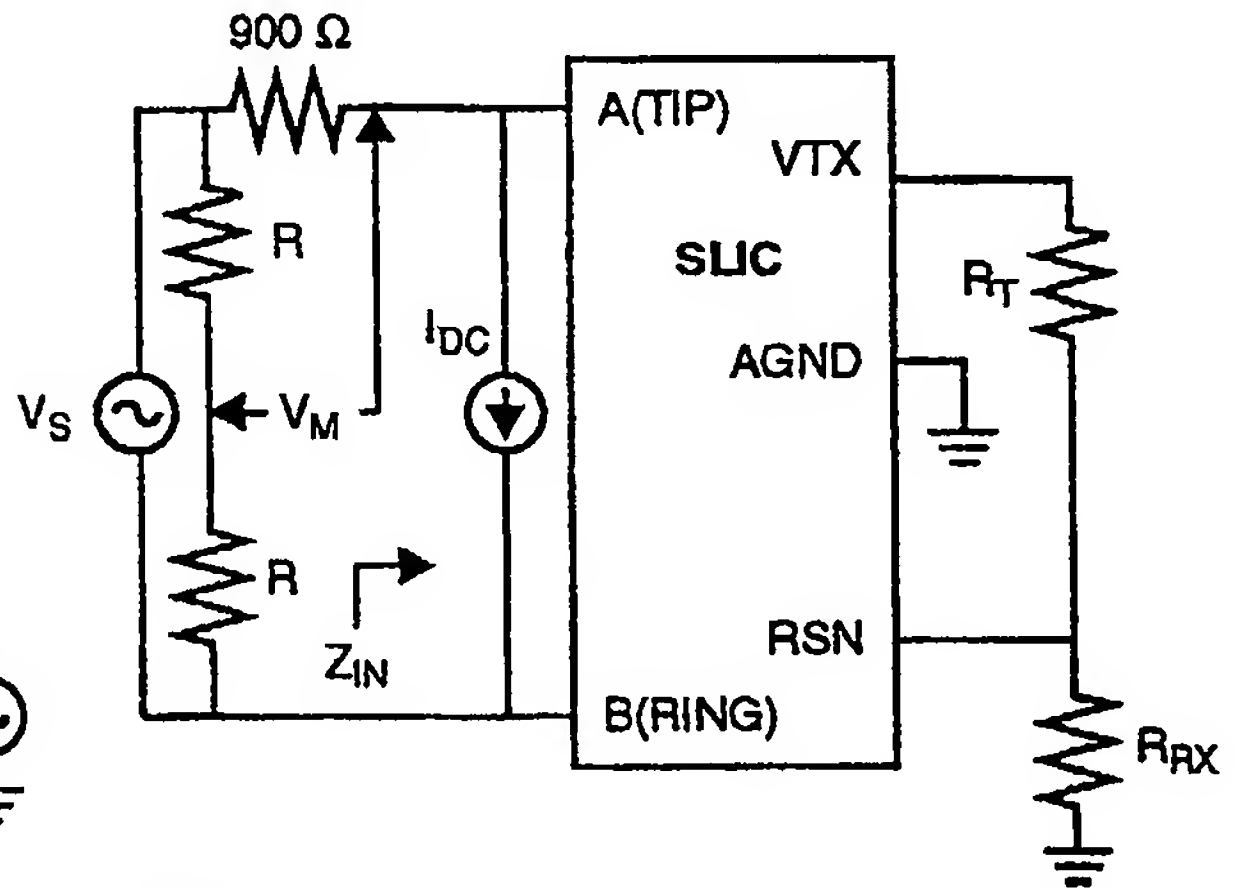
$$L-T \text{ Long. Bal.} = 20 \log (V_{AB} / V_L)$$

$$L-4 \text{ Long. Bal.} = 20 \log (V_{TX} / V_L)$$

S2 Closed, S1 Open:

$$4-L \text{ Long. Sig. Gen.} = 20 \log (V_L / V_{RX})$$

C. Longitudinal Balance



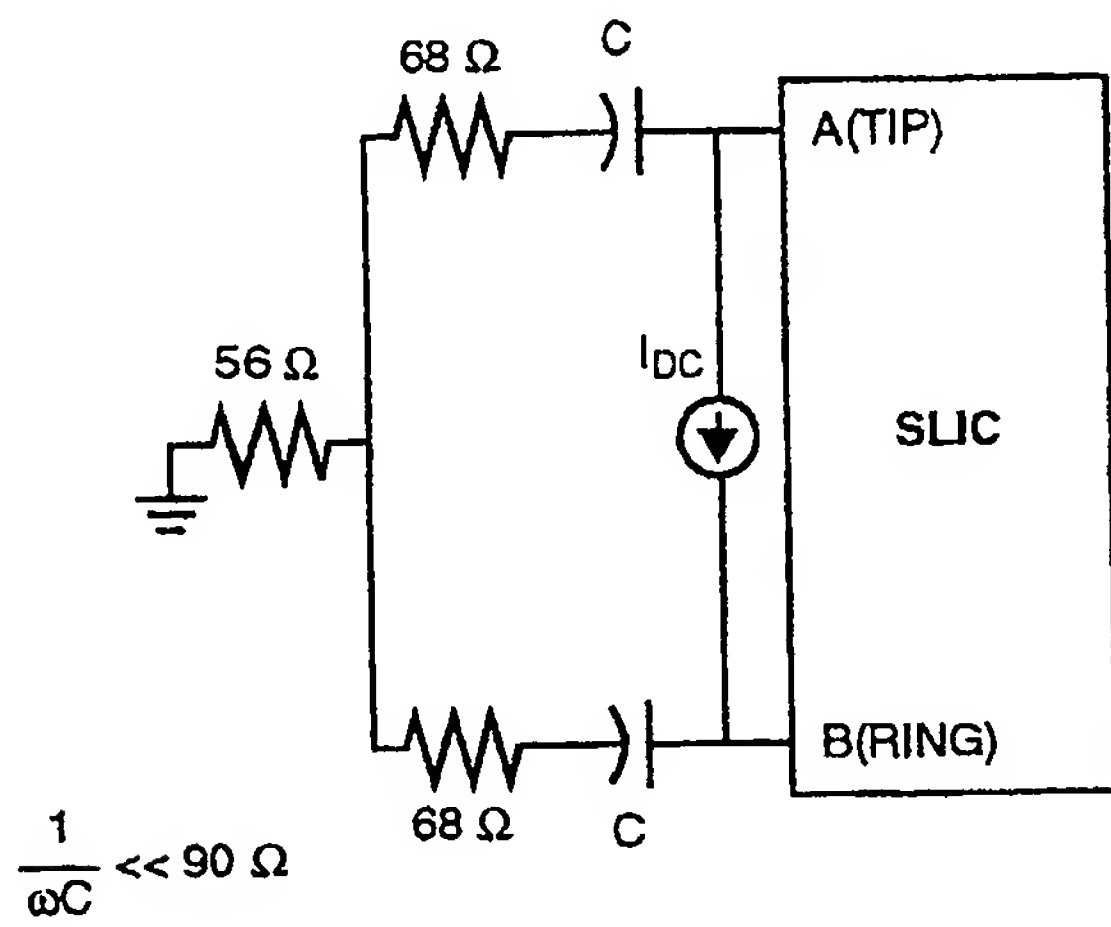
Note:

$Z_D$  is the desired impedance (e.g., the characteristic impedance of the line).

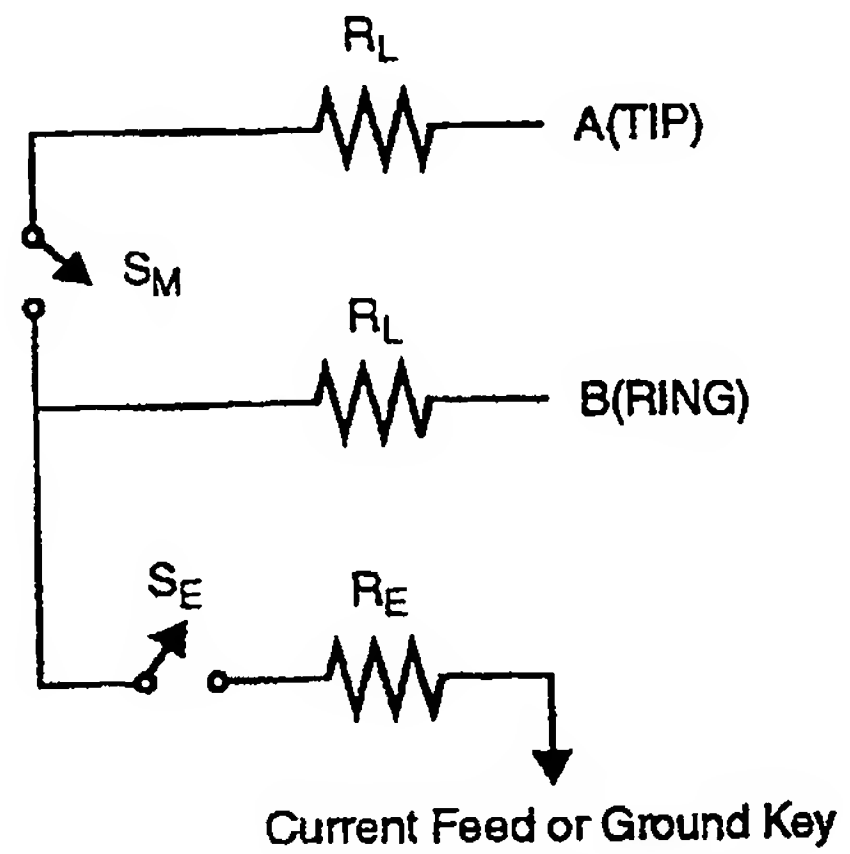
$$R_L = -20 \log (2 V_M / V_S)$$

D. Two-Wire Return Loss Test Circuit

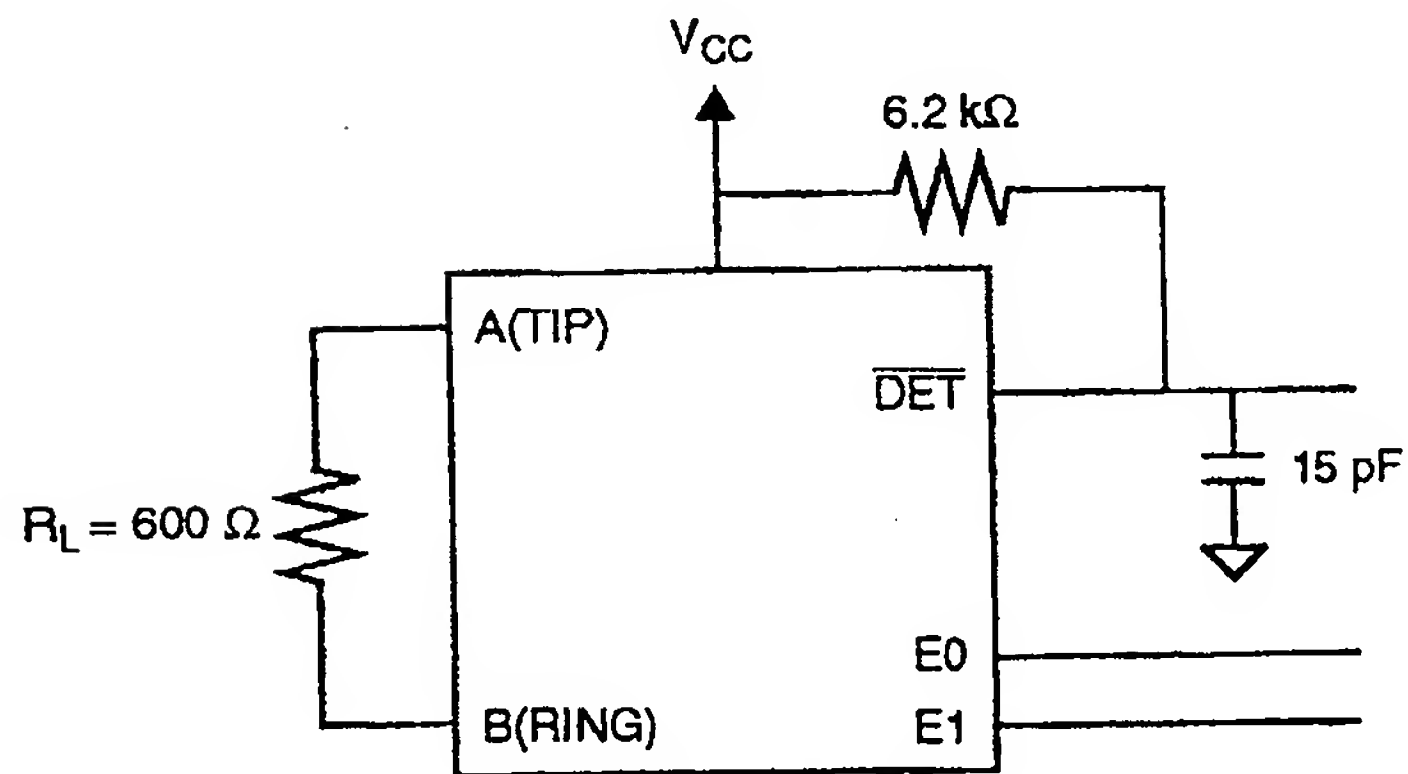
TEST CIRCUITS (continued)



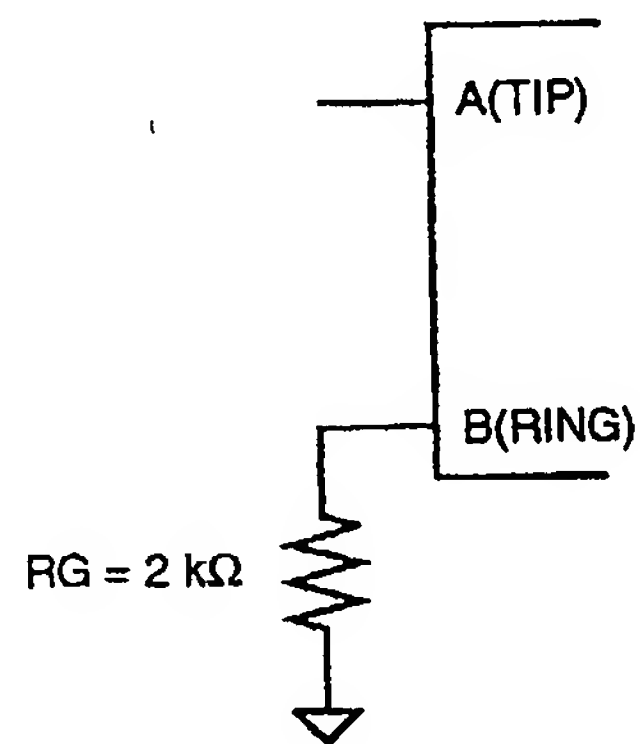
E. Single-Frequency Noise



F. Ground-Key Detection



G. Loop-Detector Switching



H. Ground-Key Switching

**REVISION SUMMARY****Revision B to Revision C**

- Minor changes to the data sheet style and format were made to conform to AMD standards.
- Connection Diagrams—Changed pin 29 from TP to RSVD in the Am79534 diagram.

**Revision C to Revision D**

- In Table 1, SLIC Decoding, the Open Circuit state of 001 was changed to 000.
- In Pin Description table, inserted/changed TP pin description to: "Thermal pin. Connection for heat dissipation. Internally connected to substrate (QBAT). Leave as open circuit or connected to QBAT. In both cases, the TP pins can connect to an area of copper on the board to enhance heat dissipation."
- Minor changes to the data sheet style and format were made to conform to AMD standards.

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